WHAT IS CLAIMED IS:

1. A non-volatile memory cell comprising:

a device isolation layer disposed in a substrate to define an active region;

a floating gate disposed over the active region and comprised of a plurality of first conductive patterns and a plurality of second conductive patterns which are alternately stacked; and

a first insulation layer interposed between the floating gate and the active region, wherein one of the first and second conductive patterns protrudes to form concave and convex shaped sidewalls of the floating gate.

2. The non-volatile memory cell of claim 1, wherein one of the first and second conductive patterns is formed of doped polysilicon layers and the other of the first and second conductive patterns is formed of doped silicon germanium layers.

3. The nonvolatile memory cell of claim 2, wherein the doped polysilicon layers protrude to form convex portions of the sidewalls of the floating gate and the doped silicon germanium layers forms concave portion of the sidewalls of the floating gate.

4. The non-volatile memory cell of claim 1, further comprising:

a control gate electrode disposed over the floating gate and crossing over the active region; and

a gate interlayer dielectric pattern disposed between the control gate electrode and the floating gate,

wherein the gate interlayer dielectric pattern and the control gate electrode are disposed over a top surface and the concave and convex sidewalls of the floating gate.

5. The non-volatile memory cell of claim 4, further comprising impurity diffusion layers formed in the active region at sides of the control gate electrode.

6. The non-volatile memory cell of claim 4, further comprising:

a selection gate pattern crossing over the active region at one side of the control gate electrode;

a floating impurity diffusion layer disposed in the active region between the selection gate pattern and the control gate electrode; and

an impurity diffusion layer respectively formed in the active region that is beside the selection gate pattern and opposite to one side of the floating impurity diffusion layer, and in the active region that is

beside the floating gate and opposite another side of the floating impurity diffusion layer,

wherein a portion of the floating impurity diffusion layer overlaps a portion of the floating gate.

7. The non-volatile memory cell of claim 6, further comprising:

a tunnel window region including a predetermined bottom region of the floating gate and the active region thereunder; and

a second insulation layer disposed between the floating gate and the active region in the tunnel window region,

wherein the tunnel window region is disposed in the overlapping region of the floating gate and the floating impurity diffusion layer, and the second insulation layer is thinner than the first insulation layer.

8. The non-volatile memory cell of claim 6, wherein the selection gate pattern comprises a first selection gate electrode, a selection gate dielectric pattern and a second selection gate electrode,

wherein the first selection gate electrode is formed of the same material layer as the floating gate, the selection gate dielectric pattern is formed of the same material layer as the gate interlayer dielectric pattern, and the second selection gate electrode is formed of the same material layer as the control gate electrode.

9. A method of forming a non-volatile memory cell comprising:

forming a device isolation layer in a semiconductor substrate to define an active region;

forming a first insulation layer over the active region;

forming a gate conductive layer over an entire surface of the semiconductor substrate with the first insulation layer, wherein the gate conductive layer comprises a plurality of first conductive layers and second conductive layers that are alternately stacked; and

forming a floating gate with concave and convex sidewalls by applying a patterning process including an isotropic etching of the gate conductive layer,

wherein the isotropic etching has etch selectivity with respect to the first and second conductive layers.

10. The method of claim 9, wherein one of the first and second conductive layers is formed of a doped polysilicon layer, and the other of the first and second conductive layers is formed of a doped silicon germanium layer.

11. The method of claim 10, wherein the isotropic etching is performed by dry etching using etch gas that includes HeO_2,

wherein the etch gas etches the doped silicon germanium layer faster than the doped polysilicon layer.

12. The method of claim 10, wherein the doped polysilicon layer and the doped silicon germanium layer are doped using an in-situ method.

13. The method of claim 9, further comprising a step of forming a gate interlayer dielectric pattern and a control gate electrode over the floating gate,

wherein the gate interlayer dielectric pattern and the control gate electrode are formed on a top surface and on the concave and convex sidewalls of the floating gate.

14. The method of claim 13, wherein the step of forming the floating gate, the gate interlayer dielectric pattern, and the control gate electrode comprises:

forming a preliminary gate conductive pattern by patterning the gate conductive layer using an anisotropic etching;

forming a gate conductive pattern having concave and convex sidewalls by etching the sidewalls of the preliminary gate conductive pattern using an isotropic etching process;

sequentially forming a gate interlayer dielectric layer and a control gate conductive layer on an entire surface of the semiconductor substrate with the gate conductive pattern; and

successively patterning the control gate conductive layer, the gate interlayer dielectric layer and the gate conductive pattern to form a floating gate, a gate interlayer dielectric pattern and a control gate electrode that are sequentially stacked, wherein the control gate electrode crosses over the active region.

15. The method of claim 14, further comprising a step of forming an impurity diffusion layer in the active region at both sides of the control gate electrode after forming the control gate electrode.

16. The method of claim 13, further comprising a step of forming a selection gate pattern that crosses over the active region at one side of the control gate electrode.

17. The method of claim 16, wherein the steps of forming the floating gate, the gate interlayer dielectric pattern, the control gate electrode, and a selection gate pattern, comprise:

forming a preliminary gate conductive pattern by patterning the gate conductive layer using anisotropic etching;

forming a gate conductive pattern by isotropically etching sidewalls of the preliminary gate conductive pattern;

forming a control gate dielectric layer and a control gate conductive layer on an entire surface of the substrate with the gate conductive pattern; and

successively patterning the control gate conductive layer, the gate interlayer dielectric layer and the gate conducive pattern to form a floating gate, a gate interlayer dielectric pattern and a control gate electrode that are sequentially stacked, and simultaneously to form a selection gate pattern crossing over the active region at one side of the control gate electrode.

18. The method of claim 16, further comprising a step of forming a floating impurity diffusion layer in a predetermined region of the active region before forming the first insulation layer,

wherein the floating gate and the selection gate pattern are formed at both sides of the floating impurity diffusion layer, and

wherein a portion of the floating gate overlaps a portion of the floating impurity diffusion layer.

19. The method of claim 18, after forming the first insulation layer and before forming the gate conductive layer, further comprising:

patterning the first insulation layer to expose a predetermined region of the floating impurity diffusion layer; and

forming a second insulation layer over the exposed floating impurity diffusion layer,

wherein the second insulation layer is formed thinner than the first insulation layer, and

wherein the second insulation layer is disposed in the overlapping region of the floating gate and the floating impurity diffusion layer.

20. A non-volatile memory cell comprising:

a substrate;

an active region formed in the substrate; and

a floating gate having sidewalls formed over the active region, the sidewalls having protruding portions.

21. The non-volatile memory cell of claim 20, wherein the floating gate comprises a plurality of first conductive patterns and a plurality of second conductive patterns.

22. The non-volatile memory of claim 21, wherein one of the plurality of first conductive patterns and the plurality of second conductive patterns forms the protruding portions of the sidewalls of the floating gate.

23. The non-volatile memory of claim 20, wherein one of the plurality of first conductive patterns and the plurality of second conductive patterns is formed of doped polysilicon layers and the other of the plurality of first conductive patterns and the plurality of second conductive patterns is formed of doped silicon germanium layers.

24. The non-volatile memory of claim 23, wherein the doped polysilicon layers form the protruding portions of the sidewalls.

25. A method of forming a non-volatile memory cell comprising:

forming an active region in a semiconductor substrate; and

forming a floating gate having sidewalls over the active region, the sidewalls having protruding portions.

26. The method of claim 25, wherein the step of forming a floating gate comprises forming a plurality of first conductive patterns and a plurality of second conductive patterns.

27. The method of claim 26, wherein one of the plurality of first conductive patterns and the plurality of second conductive patterns forms the protruding portions of the sidewalls of the floating gate.

28. The method of claim 27, wherein the one of the plurality of first conductive patterns and the plurality of second conductive patterns comprise doped polysilicon layers and the other of the plurality of first conductive patterns and the plurality of second conductive patterns comprise doped silicon germanium layers.